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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re the Application of: **Kengo INOUE et al.** Group Art Unit: **2891**

Serial Number: **10/721,870** Examiner: **Caridad Everhart**

Filed: **November 26, 2003** Confirmation Number: **6083**

For: **MANUFACTURE OF SEMICONDUCTOR DEVICE HAVING STI AND SEMICONDUCTOR DEVICE MANUFACTURED**

Attorney Docket Number: **032136**
Customer Number: **38834**

**REQUEST FOR REFUND**

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

September 6, 2005

Sir:

In response to an Office Action dated January 6, 2005, Applicants filed an Amendment on April 5, 2005. Applicants note that one new dependent claim was added. Applicants requested to be charged to Deposit Account 50-2866 for $50.00 as an extra dependent claim.

A deposit charge of $ 200.00 was subsequently charged on April 11, 2005. Applicant(s) do not recognize this charge for anything that has been filed in the referenced application. A copy of the Deposit Account monthly statement dated April 29, 2005- accompanies this Request.

Applicants request that the Patent Office refund the amount of $ **150.00** to Deposit Account 50-2866. Respectfully submitted,

**WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP**

Michael J. Caridi
Registration No. 56,171
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MJC/asc
Enclosures: Deposit Account Monthly Statement of April 29, 2005
Amendment filed on April 5, 2005

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
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# MONTHLY STATEMENT OF DEPOSIT ACCOUNT

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| Account No. |
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| 502866 |
| Date |
| 4-29-05 |
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**PLEASE SEND REMITTANCES TO:**
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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**



In re the Application of: **Kengo INOUE et al.** Group Art Unit: **2825**

Serial No.: **10/721,870** Examiner: **Caridad Everhart**

Filed: **November 26, 2003** Confirmation No.: **6083**

For: **MANUFACTURE OF SEMICONDUCTOR DEVICE HAVING STI AND SEMICONDUCTOR DEVICE MANUFACTURED**

Attorney Docket Number: **032136**
Customer Number: **38834**

**RESPONSE UNDER 37 C.F.R. § 1.116**
**EXPEDITED PROCESSING REQUESTED**

**BOX AF**
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Date: April 5, 2005

Sir:

In response to the Office Action dated January 6, 2005, Applicants amend the claims as follows and submit the following remarks.

**Amendments to the Claims** begin on page 2 of this paper.

**Remarks/Arguments** begin on page 11 of this paper.

**AMENDMENTS TO THE CLAIMS:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

Claim 1 (Previously presented): A method of manufacturing a semiconductor device comprising the steps of:

(a) forming a polishing stopper layer over a surface of a semiconductor substrate;

(b) forming a trench in said semiconductor substrate by etching said stopper layer and said semiconductor substrate;

(c) forming a first liner insulating layer of silicon oxide over a surface of said semiconductor substrate exposed in said trench;

(d) forming a second liner insulating layer of silicon nitride ~~over~~ in direct contact with said first liner insulating layer, said second liner insulating layer having a thickness of 20 nm or thicker;

(e) depositing an isolation layer of silicon oxide by plasma CVD, said isolation layer burying a recess defined by said second liner insulating layer;

(f) polishing and removing an unnecessary region of said isolation layer by using said stopper layer as a polishing stopper; and

(g) etching said stopper layer.

Claim 2 (Original): The method of manufacturing a semiconductor device according to claim 1, wherein said step (e) comprises:

(e1) depositing a third liner insulating layer of silicon oxide over said second liner insulating layer by plasma CVD at a first bias; and

(e2) depositing an isolation layer of silicon oxide by plasma CVD at a second bias higher than the first bias, said isolation layer burying a recess defined by said third liner insulating layer.

Claim 3 (Original): The method of manufacturing a semiconductor device according to claim 2, wherein the first bias in said step (e1) is no bias.

Claim 4 (Original): The method of manufacturing a semiconductor device according to claim 2, wherein said step (e1) includes a step of performing pre-heating at 400 °C to 450 °C and a next step of forming said third liner insulating layer of silicon oxide.

Claim 5 (Original): The method of manufacturing a semiconductor device according to claim 2, wherein said step (e1) deposits said third liner insulating layer of silicon oxide by diode parallel plate plasma CVD.

Claim 6 (Original): The method of manufacturing a semiconductor device according to claim 2, wherein said step (e2) is executed by using an inductive coupling plasma CVD system.

Claim 7 (Original): The method of manufacturing a semiconductor device according to claim 1, further comprising after said step (d), the step of performing annealing at 1000 °C to 1150 °C.

Claim 8 (Original): The method of manufacturing a semiconductor device according to claim 1, wherein said second liner insulating layer has a tensile stress of 1.2 GPa or larger.

Claim 9 (Original): The method of manufacturing a semiconductor device according to claim 1, wherein the plasma CVD is high density plasma CVD.

Claim 10 (Original): A method of manufacturing a semiconductor device comprising the steps of:

(a) forming a polishing stopper layer over a surface of a semiconductor substrate;

(b) forming a trench in said semiconductor substrate by etching said stopper layer and said semiconductor substrate;

(c) forming a first liner insulating layer of silicon oxide over a surface of said semiconductor substrate exposed in said trench;

(d) forming a second liner insulating layer of silicon nitride over said first liner insulating layer;

(e1) depositing a third liner insulating layer of silicon oxide over said second liner insulating layer by plasma CVD at a first bias;

(e2) depositing an isolation layer of silicon oxide by plasma CVD at a second bias higher than the first bias, said isolation layer burying a recess defined by said third liner insulating layer;

(f) polishing and removing an unnecessary region of said isolation layer by using said stopper layer as a polishing stopper; and

(g) etching said stopper layer.

Claim 11 (Original): The method of manufacturing a semiconductor device according to claim 10, wherein the first bias in said step (e1) is no bias.

Claim 12 (Original): The method of manufacturing a semiconductor device according to claim 10, wherein said step (e1) includes a step of performing pre-heating at 400 °C to 450 °C and a next step of forming said third liner insulating layer of silicon oxide.

Claim 13 (Original): The method of manufacturing a semiconductor device according to claim 10, wherein said step (e1) deposits said third liner insulating layer of silicon oxide by diode parallel plate plasma CVD.

Claim 14 (Original): The method of manufacturing a semiconductor device according to claim 10, wherein said step (e2) is executed by using an inductive coupling plasma CVD system.

Claim 15 (Original): The method of manufacturing a semiconductor device according to claim 10, further comprising after said step (d), a step of performing annealing at 1000 °C to 1150 °C.

Claim 16 (Original): The method of manufacturing a semiconductor device according to claim 10, wherein said second liner insulating layer has a tensile stress of 1.2 GPa or larger.

Claim 17 (Original): The method of manufacturing a semiconductor device according to claim 10, wherein the plasma CVD is high density plasma CVD.

Claim 18 (Original): The method of manufacturing a semiconductor device according to claim 10, wherein the second liner insulating layer has a thickness of 8 nm or thinner.

Claim 19 (Original): A method of manufacturing a semiconductor device comprising the steps of:

(a) forming a polishing stopper layer over a surface of a semiconductor substrate;

(b) forming a trench in said semiconductor substrate by etching said stopper layer and said semiconductor substrate;

(c) forming a first liner insulating layer of silicon oxide over a surface of said semiconductor substrate exposed in said trench;

(d) forming a second liner insulating layer of carbon-containing silicon nitride over said first liner insulating layer;

(e) depositing an isolation layer of silicon oxide by plasma CVD, said isolation layer burying a recess defined by said second liner insulating layer;

(f) polishing and removing an unnecessary region of said isolation layer by using said stopper layer as a polishing stopper; and

(g) etching said stopper layer.

Claim 20 (Original): The method of manufacturing a semiconductor device according to claim 19, wherein said step (d) deposits the carbon-containing silicon nitride layer by chemical

vapor deposition using organic silicon source gas, or a combination of silicon source gas and an organic gas.

Claim 21 (Original): The method of manufacturing a semiconductor device according to claim 19, wherein said step (d) deposits the carbon-containing silicon nitride layer by chemical vapor deposition using bis-tertial butylaminosilane (BTBAS) and ammonia as source gas.

Claim 22 (Original): The method of manufacturing a semiconductor device according to claim 21, wherein said step (d) is carried out at a substrate temperature of 550 °C - 580 °C.

Claim 23 (Original): The method of manufacturing a semiconductor device according to claim 19, wherein said step (g) is carried out under such condition that etching rate for the second liner insulating layer is smaller than etching rate for the silicon nitride layer of said stopper layer.

Claim 24 (Original): A semiconductor device comprising:

a semiconductor substrate;

a trench formed in said semiconductor substrate, and defining active regions;

a first liner layer of silicon oxide covering surface of each said trench;

a second liner layer of carbon-containing silicon nitride formed over said first liner layer;

an isolation region of silicon oxide formed over said second liner layer and filling said trench; and

a p-channel MOS transistor formed in one of said active regions.

Claim 25 (Original): The semiconductor device according to claim 24, wherein said second liner layer has a tensile stress larger than 1.2 GPa.

Claim 26 (Original): The semiconductor device according to claim 24, wherein said second liner layer does not form a divot relative to surface of the semiconductor substrate.

Claim 27 (Original): The semiconductor device according to claim 24, further comprising an n-channel MOS transistor formed in another of said active regions, forming CMOS configuration with said p-channel MOS transistor.

Claim 28 (Original): The semiconductor device according to claim 24, further comprising:

interlevel insulating layers covering said CMOS configuration, and having low UV absorption coefficient;

multi-layer wiring formed in said interlevel insulating layers.

Claim 29 (Previously presented): A semiconductor device comprising:

a semiconductor substrate;

a trench formed in said semiconductor substrate, and defining active regions;

a first liner layer of silicon oxide covering surface of each said trench;

a second liner layer of silicon nitride formed over said first liner layer by using a source gas which leaves carbon in product silicon nitride;

an isolation region of silicon oxide formed over said second liner layer and filling said trench; and

a p-channel MOS transistor formed in one of said active regions.

Claim 30 (Previously presented): The semiconductor device according to claim 29, wherein said second liner layer has a tensile stress larger than 1.2 GPa.

Claim 31 (Previously presented): The semiconductor device according to claim 29, wherein said second liner layer does not form a divot relative to surface of the semiconductor substrate.

Claim 32 (Previously presented): The semiconductor device according to claim 29, further comprising an n-channel MOS transistor formed in another of said active regions, forming CMOS configuration with said p-channel MOS transistor.

Claim 33 (Previously presented): The semiconductor device according to claim 29, further comprising:

interlevel insulating layers covering said CMOS configuration, and having low UV absorption coefficient;

multi-layer wiring formed in said interlevel insulating layers.

Claim 34 (Previously presented): The semiconductor device according to claim 24, wherein said source gas is BTBAS.

Claim 35 (New): The method of manufacturing a semiconductor device according to claim 1, further comprising said second liner insulating layer having a thickness of greater than 20 nm.

## REMARKS

Claims 1-35 are pending. Claims 2-6, 8, 25 and 30 stand objected to as being dependent on rejected base claims. Claims 10-18 are allowed. Claims 1, 7, 9, 19-24, 26-29 and 31-34 are rejected. Claim 35 has been added herein. Support for the new claim is based on original claim 1.

**Applicants' Response to Claim Rejections under 35 U.S.C. § 102(e)**

Claims 1 and 9 stand rejected under 35 U.S.C. 102(e) as being anticipated by Heo, et al. (US 2004/0171271A1). Applicants respectfully traverse on the basis that claim 1 is not anticipated within the meaning of §102, because each and every limitation is not taught in the cited reference. Specifically, the limitation that the silicon nitride layer has a thickness of 20 nm or thicker is not present in Heo et al. Heo et al. teaches the use of a thinner silicon nitride layer to minimize the effect of the nitride layer with respect to the aspect ratio of a narrower trench.

The Office Action asserts that Heo et al. discloses a silicon nitride layer of 20 nm or greater, referencing paragraph [0035]. However, applicants respectfully submit that there is no such disclosure in the paragraph. Rather, Heo et al. teaches a lower thickness for the silicon nitride layer 150. Heo et al. states in paragraph [0035] that "... the nitride liner 150 is ... formed to a thickness ...about 30 to 140 Å." Since 1 nm=10Å, the cited thickness is from about 3 to 14 nm, smaller than 20 nm. This thickness is taught to prevent diffusion of impurities while also minimizing the effect of the silicon nitride layer with respect the aspect ratio of the first trench 131 (i.e. narrower trenches).

Applicants further submit that the claimed limitation would not be inherent or obvious in light of the disclosures of Heo et al. Specifically, as set forth above, Heo et al. teaches away

from utilizing a silicon nitride layer greater than 14 nm. A greater thickness is taught as possibly disrupting the formation of the isolation region in the first trench 131. See paragraph [0035].

However, the present invention teaches toward a greater thickness to obtain a process free of tear-off by utilizing the silicon nitride layer in the trench. Specifically, the influence of the thickness of the silicon nitride liner layer was studied by the present inventors. Their research indicates that no tear-off occurs if the thickness of the silicon nitride liner layer is set to 20 nm or thicker. See page 11, lines 8-11. There is no such disclosure in Heo et al. and Heo et al. teaches toward a thinner silicon nitride layer. Applicants respectfully submit that the rejection of claim 9 is likewise addressed by nature of the claims dependency to claim 1. Applicants, in light of the above remarks, respectfully request favorable reconsideration.

**Applicants' Response to Claims Rejections under 35 U.S.C. § 103(a)**

Claims 7, 19-24, 26-29 and 31-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heo et al. as applied to claim 1 and further in view of Laxman, et al. (US 5,874,368). In regard to claim 7, the rejection is traversed as above by nature of the claim's dependency to claim 1. Further, Applicant's claim 7 recites an annealing step at 1000°C to 1150°C, after depositing silicon nitride liner. The Office Action points to Laxman as disclosing this limitation. However, Laxman recites a deposition temperature including 1000°C at the highest, not an anneal step at 1000°C to 1150°C, after deposition. See Column 2, lines 37-38.

In regard to independent claims 19, 24, and 29, they require carbon present in the silicon nitride liner as a limitation. The Office Action has added Laxman et al. for its apparent teaching of a silicon nitride which contains carbon. The Office Action maintains that because organic source material is used, carbon will be incorporated into the nitride layer.

Applicants respectfully submit that Laxman et al. is teaching away from a silicon nitride which has a carbon contaminate. Laxman specifically states that "analogous aminosilanes... do not deposit carbon free films at such low temperatures." See Col. 4, lines 19-23. See also column 4, lines 23-36 (the claimed silane forms stable leaving groups which do not cause contamination). The third listed advantage of Laxman et al. at column 4, lines 45-47 states:

> 3) The precursor does not contain direct Si – C bonds, and
> the resulting silicon nitride films were carbon free, as
> indicated by auger spectroscopy.

The Office Action cites to Table 1 which discloses a number of precursor materials as comparative examples to the taught invention. The comparative examples are considered inferior by Laxman et al. because they result in carbon contamination.

In short, one skilled in the art reviewing Laxman et al. would not be motivated to combine the comparative examples with the teachings of Heo et al. Laxman et al. clearly teaches away from carbon contamination. The actual invention of Laxman et al. combined with Heo et al. would not result in the present invention of claims 19, 24, and 29 because these claims require carbon in the silicon nitride layer.

In other words, the teachings of Laxman are directly contrary to the teachings of the present application. According to the applicant's invention, the carbon-containing silicon nitride film has the following merits: (1) there are less charge trap sites so that the film is hardly charged; (2) the carbon-containing silicon nitride has good adhesion to the underlying silicon oxide film, and peel-off can hardly occur; (3) tensile stress of the silicon nitride is increased to increase the transistor characteristics; and (4) it has strong resistance against boiling phosphoric acid, and there is less possibility of causing divot. These merits are confirmed in comparison

with the carbon-free silicon nitride film. Hence, applicants respectfully submit that the present invention of claims 19, 24 and 29 and there respective dependent claims would not be obvious over Heo et al. as applied to claim 1 and further in view of Laxman, et al. (US 5,874,368). Laxman et al. does not teach a carbon-containing silicon nitride film as required by applicants' claims, but in fact teaches away from it. Wherefore, favorable reconsideration is respectfully requested.

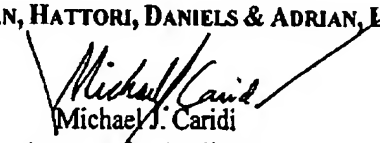
In view of the aforementioned amendments and accompanying remarks, Applicants submit that that the claims, as herein amended, are in condition for allowance. Applicants request such action at an early date.

If the Examiner believes that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney to arrange for an interview to expedite the disposition of this case.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP



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MJC/mlj

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re the Application of: **Kengo INOUE et al.** Group Art Unit: **2891**

Serial No.: **10/721,870** Examiner: **Caridad Everhart**

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Attorney Docket Number: **032136**
Customer Number: **38834**

**AMENDMENT UNDER 37 C.F.R. § 1.111**

Mail Stop: Amendment
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Date: August 8, 2005

Sir:

This paper is filed in response to the Office Action dated May 9, 2005.

**Amendments to the Claims** begin on page 2 of this paper.

**Remarks/Arguments** begin on page 12 of this paper.